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CLEAN VERSION OF PENDING CLAIMS

ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

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Claims 1-9, 33-35, 46, 48-50, 59-61, 63 and 64, as of May 15, 2002 (Date of Response to Final Office Action after CPA).

1. An asynchronously-accessible storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode; and

circuitry operable in either a burst mode or a pipelined mode coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device in either mode.

2. The asynchronously-accessible storage device of Claim 1 wherein the burst mode and the pipelined mode are extended data out modes of operation.

3. The asynchronously-accessible storage device of Claim 1 wherein the pipelined mode is an extended data out mode.

4. The asynchronously-accessible storage device of Claim 1 wherein the burst mode is an extended data out mode.

5. The asynchronously-accessible storage device of Claim 1 wherein the piplined/burst mode circuitry includes a buffer, the buffer for storing an address.

6. The asynchronously-accessible storage device of Claim 5 wherein the piplined/burst mode circuitry includes at least one counter for incrementing the address.

7. (Once Amended) The asynchronously-accessible storage device of Claim 1 wherein the pipelined/burst mode circuitry is coupled for reading an external address.

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8. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes a buffer for storing the external address.

9. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes mutliplexed devices for providing an internally generated address to the storage device.

33. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device;

selecting between outputting information from the storage device and inputting information to the storage device;

obtaining a second address to the storage device; and

asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

34. The method of Claim 33, further comprising switching between the burst mode and the pipelined mode.

35. The method of Claim 33, wherein the second address is an external address.

46. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipelined mode of operation;

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the pipelined mode of operation;

switching modes to a burst mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation; and

generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation.

48. The method of Claim 46 wherein the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

49. The method of Claim 46 wherein the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

50. A system comprising:

a microprocessor;

a memory, coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory; and

a system clock coupled to the microprocessor.

59. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

receiving a burst/pipeline signal;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;

obtaining a second address to the storage device; and

accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

60. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

receiving a burst/pipeline signal;

selecting between outputting information from the storage device and inputting information to the storage device;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;

obtaining a second address to the storage device; and

asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

61. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipeline mode of operation;

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation;

switching modes to the burst mode of operation;

providing an initial external address associated with asynchronously accessing the

asynchronously-accessible memory device in the pipelined mode of operation; and

while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation.

63. A storage device, comprising:

an array of memory cells;

mode circuitry for receiving a burst/pipeline signal; and

operation circuitry operable in a burst or a pipeline mode of operation depending upon the burst/pipeline signal, the operation circuitry switchable between burst and pipeline modes of operation.

64. A memory circuit, comprising:

an array of memory cells;

burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation of the memory circuit; and

mode circuitry capable of operation in either a burst mode or a pipeline mode of operation, and switchable between burst and pipeline modes of operation.